

A Comparative Application of Performance of the SEPIC Converter Using PI, PID and Fuzzy Logic Controllers for PMDC Motor Speed Analysis

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Abstract—DC converters are widely used in industrial area. SEPIC converter is a suitable converter when the input voltage has got wide variations around the rated voltage. In this study presents an analysis of the dynamic performance on DC-DC SEPIC (Single Ended Primary Inductor Converter) converter which is driving Permanent Magnet DC Motor (PMDC Motor) with PI, PID and fuzzy logic controller implementation. One of the applications in which source side variations are wide is DC Motor applications. Therefore, importance is given to source side disturbance of SEPIC converter. Hence in this paper, a PID controller and fuzzy logic controller have been implemented to improve the dynamic and steady state performance of the SEPIC converter when source voltage is subjected to wide variations keeping the output voltage at a constant value at steady state. Simulation results have been obtained using MATLAB/SIMULINK. The percentage overshoot, rise time and settling time have been compared and analyzed.

Keywords—DC-DC converter, Fuzzy Logic controller (FLC), Proportional Integral (PI) control, Proportional Integral Derivative (PID) control, SEPIC converter, Permanent Magnet DC Motor (PMDC Motor).

I. INTRODUCTION

In recent years, with the rapid development of industry, electric power, and this power can be controlled by the Power Electronics Circuit was committed, the need for increased rapidly. AC-DC and DC-DC Motor Speed Control Units, Uninterruptible Power Supplies, Battery Chargers, Switch Mode AC-DC Power Supplies, Static devices such as voltage regulators, providing electrical power feeding the load that needs major industrial power electronics applications [1].

A DC-DC converters are widely used in regulated switch-mode dc power supplies and in dc motor drive applications. Often the input to the converters is an unregulated dc voltage, which is obtained by rectifying the line voltage, and therefore it will fluctuate due to changes in the line voltage magnitude [2].

In many industrial applications DC voltage value instead of a fixed value of the DC voltage is needed at different levels. Constant DC voltage level, different DC voltage levels are used to convert DC converter circuits. Input-output voltage values are used differently depending on the structure of the DC converter circuit. The first thing to be considered when selecting the converter structure input and output voltage values. For example, according to the input voltage value of the output voltage increases when the desired value is higher when using the structure-type DC converter, the output voltage value of the input voltage is lower than the value used when necessary to reduce such DC converter structure [3].

DC-DC converters are many different types. They all have advantages and disadvantages relative to each other. Some of the voltage converters to reduce some of the others in enhancing and increasing the reduction is used. DC-DC converters with fuzzy logic control algorithm incorporating all kinds of engineering applications can be applied successfully. Fuzzy logic control DC-DC converter and has a better performance as well as reduced costs. In parallel with the development of digital technology and digital control, the application of fuzzy logic in proportion to the power transformer developed [4].

II. SEPIC CONVERTERS

The single-ended primary inductance converter (SEPIC) is a DC/DC-converter topology that provides a positive regulated output voltage from an input voltage that varies from above to below the output voltage. It operates in continuous, discontinuous, or boundary conduction mode. SEPIC is controlled by the duty cycle of the control transistor. SEPICs are useful in applications in which a battery voltage can be above and below that of the regulator's intended output. As with other switched mode power supplies specifically DC-to-DC converters, the SEPIC exchanges energy between the capacitors and inductors in order to convert from one voltage to another. A simple circuit diagram of a SEPIC converter is shown in Fig. 1., consisting of a coupling capacitor, C_1 and output capacitor, C_2 ; coupled inductors L_1 and L_2 and diode.

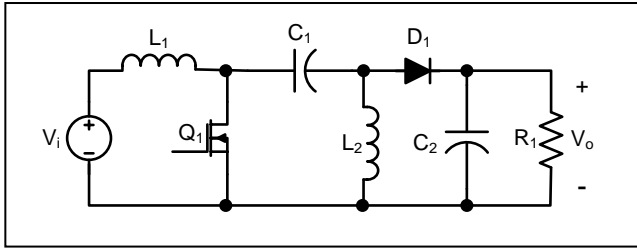


Fig. 1. Simple circuit diagram of SEPIC converter

Fig. 2 shows the circuit when the power switch is turned on. The first inductor, L_1 , is charged from the input voltage source during this time. The second inductor takes energy from the first capacitor, and the output capacitor is left to provide the load current. No energy is supplied to the load capacitor during this time. Inductor current and capacitor voltage polarities are also marked.

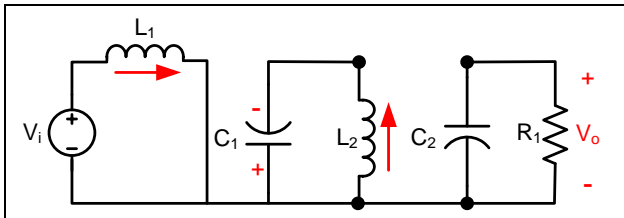


Fig. 2. SEPIC converter when switched ON

When the power switch is turned off, the first inductor charges the capacitor C_1 and also provides current to the load, as shown in Fig. 3. The second inductor is also connected to the load during this time. The output capacitor sees a pulse of current during the off time, making it inherently noisier than a buck converter [5].

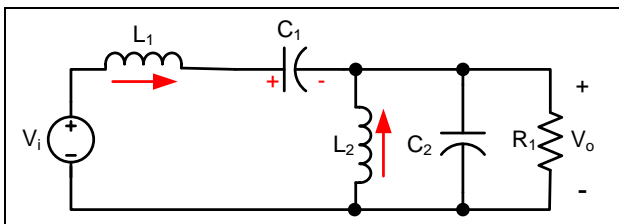


Fig. 3. SEPIC converter when switched OFF

The formulae of duty cycles are given as follows:

$$D_{\max} = \frac{V_0 + V_D}{V_{i(\min)} + V_0 + V_D} \quad (1)$$

$$D_{\min} = \frac{V_0 + V_D}{V_{i(\max)} + V_0 + V_D} \quad (2)$$

For determining the inductance is to allow the peak-to-peak ripple current to be approximately 40% of the maximum input current at the minimum input voltage. The ripple current flowing in equal value inductors L_1 and L_2 is given by,

$$\Delta I_L = I_i \%40 = I_0 \frac{V_0 \%40}{V_{i(\min)}} \quad (3)$$

The inductor value is calculated by,

$$L_1 = L_2 = L = \frac{V_{i(\min)}}{\Delta I_L f_{sw}} D_{\max} \quad (4)$$

where f_{sw} is the switching frequency and D_{\max} is the duty cycle at the minimum V input. The peak current in the inductor, to ensure the inductor does not saturate, is given by,

$$I_{L1\text{ peak}} = I_0 \frac{V_0 + V_D}{V_{i(\min)}} \left(1 + \frac{\%40}{2}\right) \quad (5)$$

$$I_{L2\text{ peak}} = I_0 \frac{V_0 + V_D}{V_{i(\min)}} \left(1 + \frac{\%40}{2}\right) \quad (6)$$

If L_1 and L_2 are wound on the same core, the value of inductance in the equation above is replaced by $2L$ due to mutual inductance. The inductor value is calculated by,

$$L'_1 = L'_2 = \frac{L}{2} = \frac{V_{i(\min)}}{2\Delta I_L f_{sw}} D_{\max} \quad (7)$$

Power Switch Selection, the parameters governing the selection of the MOSFET are the minimum threshold voltage $V_{th(\min)}$, the on resistance $R_{DS(ON)}$, gate-drain charge Q_{GD} and the maximum drain to source voltage, $V_{DS(\max)}$. Logic level or sublogic-level threshold switch' should be used based on the gate drive voltage. The peak switch voltage is equal to $V_{in} + V_{out}$. The peak switch current is given by,

$$I_{Q1\text{ peak}} = I_{L2\text{ peak}} + I_{L2\text{ peak}} \quad (8)$$

The RMS current through the switch is given by,

$$I_{Q1\text{ rms}} = I_0 \sqrt{\frac{(V_0 + V_{i(\min)} + V_0)(V_0 + V_D)}{V_{i(\min)}^2}} \quad (9)$$

$$P_{Q1\text{ rms}} = I_{Q1\text{ rms}}^2 R_{DS(ON)} D_{\max} + (V_{i(\min)} + V_0) I_{Q1\text{ peak}} \frac{Q_{DO} f_{sw}}{I_G} \quad (10)$$

P_{Q1} , the total power dissipation for MOSFETs includes conduction loss (as shown in the first term of the above equation) and switching loss as shown in the second term. I_G is the gate drive current. The $R_{DS(ON)}$ value should be selected at maximum operating junction temperature and is typically given in the MOSFET data sheet. Ensure that the conduction losses plus the switching losses do not exceed the package ratings or exceed the overall thermal budget.

Input Capacitor Selection: The SEPIC has an inductor at the input. Hence, the input current waveform is continuous and triangular. The inductor ensures that the input capacitor sees fairly low ripple currents. The RMS current in the input capacitor is given by,

$$I_{C_{in\text{ rms}}} = \frac{\Delta I_L}{\sqrt{12}} \quad (11)$$

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not

so critical in a SEPIC application, a 10 if or higher value, good quality capacitor would prevent impedance interactions with the input supply.

Output Capacitor Selection: When the power switch Q_1 is turned on the inductor is charging the output current is supplied by the output capacitor. The RMS current in the output capacitor is,

$$I_{C_{0,rms}} = I_0 \sqrt{\frac{V_0 + V_D}{V_{i,min}}} \quad (12)$$

The ESR, ESL and the bulk capacitance of the output capacitor directly control the output ripple. Assume half of the ripple is caused by the ESR and the other half is caused by the amount of capacitance.

$$ESR \leq \frac{V_{ripple} \%50}{I_{L_1,peak} + I_{L_2,peak}} \quad (13)$$

$$C_0 = \frac{I_0 D}{\%50 V_{ripple} f_{sw}} \quad (14)$$

In surface mount applications, tantalum, polymer electrolytic and polymer tantalum, or multi-layer ceramic capacitors are recommended at the output [6].

SEPIC Coupling Capacitor Selection: The selection of SEPIC capacitor, C_s , depends on the RMS current, which is given by,

$$I_{C_{0,rms}} = I_0 \sqrt{\frac{V_0 + V_D}{V_{i,min}}} \quad (15)$$

The SEPIC capacitor must be rated for a large RMS current relative to the output power. The voltage rating of the SEPIC capacitor must be greater than the maximum input voltage. The peak-to-peak ripple voltage on C_s ,

$$\Delta V_{cs} = \frac{I_0 D_{max}}{C_s f_{sw}} \quad (16)$$

State Space Analysis of SEPIC converter for continuous conduction mode can be done in two modes of operation. For a given network has two states in CCM, S_1 on, S_2 off and S_1 off, S_2 on, the response of the network in each state may be time weighted and averaged. The state equations can be expressed in matrix form as,

$$\dot{X} = A_1 x + B_1 u \quad (17)$$

$$Y = C_1 x + D \quad (18)$$

where X is the time derivative of the state variable vector, A_1 is the state matrix, x is the state variable vector, B_1 is the input matrix, u is the input and Y is the output. The state variables are taken as,

$$x_1 = i_{L_1} \quad (19)$$

$$x_2 = i_{L_2} \quad (20)$$

$$x_3 = i_{C_1} \quad (21)$$

$$x_4 = i_{C_2} \quad (22)$$

Mode 1: Switch S: ON ($0 < t < DT$)

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{RC_2} \end{bmatrix} \quad B_1 = \begin{bmatrix} \frac{1}{L_1} \\ L_1 \\ 0 \\ 0 \end{bmatrix} \quad (23)$$

Mode 2: Switch S: OFF ($DT < t < (1-D)T$)

$$A_2 = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & -\frac{1}{L_1} \\ 0 & 0 & 0 & -\frac{1}{L_2} \\ -\frac{1}{C_1} & 0 & 0 & 0 \\ \frac{1}{C_2} & \frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \quad B_2 = \begin{bmatrix} \frac{1}{L_1} \\ L_1 \\ 0 \\ 0 \end{bmatrix} \quad (24)$$

The state space averaged equation is given as,

$$X = [A_1 d + A_2 (1-d)]x + [B_1 d + B_2 (1-d)]u \quad (25)$$

Therefore, the large signal model is expressed as,

$$\begin{bmatrix} \dot{i}_{L_1} \\ \dot{i}_{L_2} \\ \dot{v}_{C_1} \\ \dot{v}_{C_2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{d-1}{L_1} & \frac{d-1}{L_1} \\ 0 & 0 & \frac{d}{L_2} & \frac{d-1}{L_2} \\ \frac{1-d}{C_1} & -\frac{d}{C_1} & 0 & 0 \\ \frac{1-d}{C_2} & \frac{1-d}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ L_1 \\ 0 \\ 0 \end{bmatrix} [u] \quad (26)$$

III. SYSTEM CONTROL LOOP

The SEPIC converter is controlled with a voltage mode control scheme. The PWM module is configured for SEPIC mode with an independent time-base. The DC Link voltage is measured by the voltage sensors and sent to DSP control. This value is subtracted from the voltage reference in software to obtain the voltage error.

The voltage error is then fed into a control algorithm that produces a duty cycle value based on the voltage error, previous error, and control history. The output of the control algorithm is also clamped to minimum and maximum duty cycle values for hardware protection. The voltage mode control algorithm must be executed at a fast rate in order to achieve the best transient response. Therefore, the control algorithm is executed in the ADC interrupt service routine, which is also assigned the highest priority in the UPS code [7]. A block diagram of the push-pull converter control scheme is shown in Fig. 4.

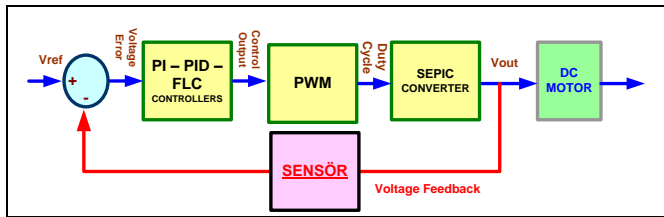


Fig. 4. A Block diagram of SEPIC voltage control loop

IV. CONTROL SYSTEMS MODELS

A. Proportional Integral (PI) Control

The control block diagram of the classical PI controller is given in Fig. 5. According to DC converter reference voltage input circuit, output voltage, is controlled by the PI controller. On activated equations are as follows. When you submit your final version, after your paper has been accepted, prepare it in two-column format, including figures and tables [8].

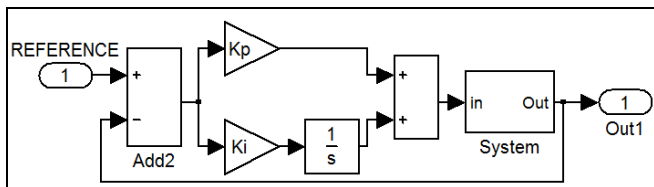


Fig. 5. PI Controller Block Diagram

B. Proportional Integral Derivative (PID) Control

The PID controller is the most common form of feedback. It was an essential element of early governors and it became the standard tool when process control emerged in the 1940s. The "textbook" version of the PID algorithm is described by equation (2).

$$u(t) = K \left(e(t) + \frac{1}{T_i} \int_0^t e(\tau) d\tau + T_d \frac{de(t)}{dt} \right) \quad (27)$$

where y is the measured process variable, r the reference variable, u is the control signal and e is the control error ($e = y_{sp} - y$). The reference variable is often called the set point. The control signal is thus a sum of three terms: the P-term (which is proportional to the error), the I-term (which is proportional to the integral of the error), and the D-term (which is proportional to the derivative of the error). The controller parameters are proportional gain K , integral time T_i , and derivative time T_d [9].

C. Fuzzy Logic Control

The first is a small steam engine as the control for fuzzy logic control was carried out by Mamdani and Assilian. Fuzzy logic control algorithm consists of a set of rules and linguistic terms to express an intuitive control for fuzzy sets and fuzzy logic to evaluate the rules used [10-11].

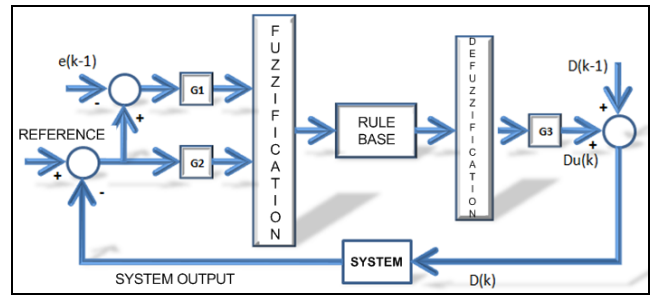


Fig. 6. FLC Controller Block Diagram

As is known, the structure of fuzzy logic controller consists of three parts. If you need a brief look at these sections, the first as "The Blur" phase, the absolute values are converted to fuzzy values. Then, fuzzy rules, fuzzy values are processed "Rule processing and decision-making" phase, and finally, "defuzzification" step, the exact result is converted to fuzzy. Fuzzy logic control system is shown in Fig. 6. [12].

V. SIMULATION OF THE FULL SYSTEM

In Fig. 7. shown the whole system, in turn, is connected to the PID and FLC. These controllers, variable speed error between the reference and the output signal audited by the push-pull converter is PMDC motor actual speed with PWM method determines the position of the MOSFET or ideal switches. SEPIC converter determines the output voltage of the switch position. This voltage determines the speed of the motor.

VI. CONCLUSION

In MATLAB / Simulink programming, the variable reference speed applied to PI, PID and Fuzzy based control have been made, the SEPIC converter output speed PI was observed for PID and fuzzy controlled systems. PI controlled system simulation results are shown in Figure 8, Figure 9 and Figure 10.

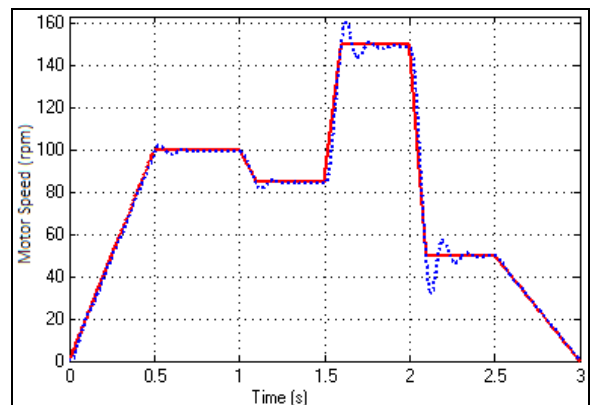


Fig. 8. SEPIC converter with PI controller 0s - 3s response

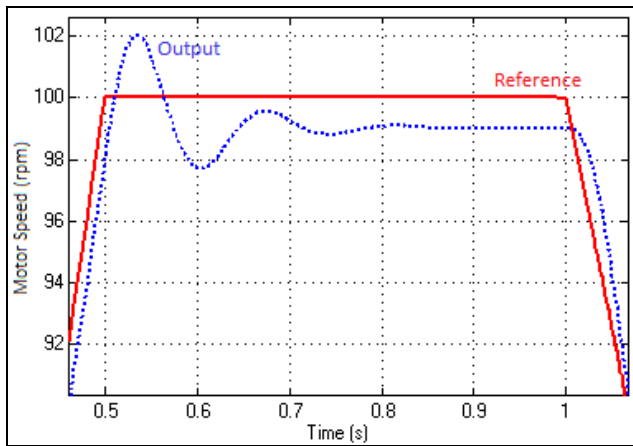


Fig. 9. SEPIC converter with PI controller 0.5s - 1s response

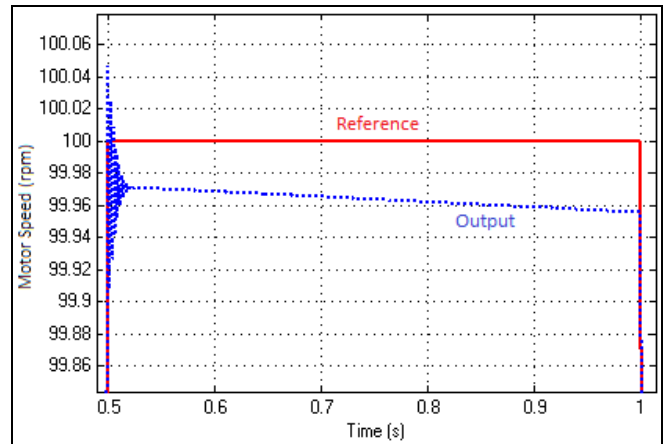


Fig. 12. SEPIC converter with PID controller 0.5s - 1s response

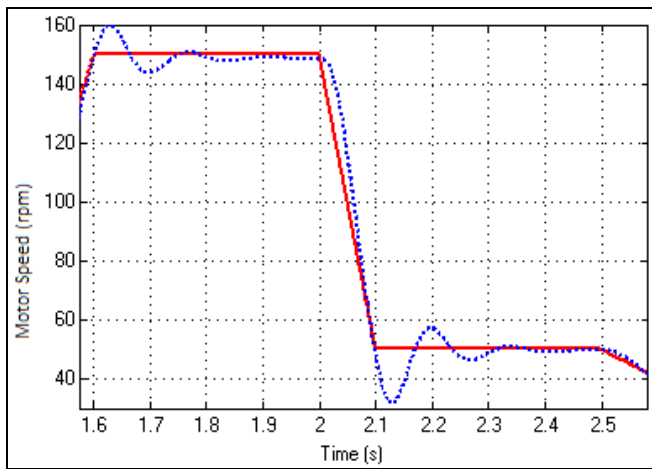


Fig. 10. SEPIC converter with PI controller 1.6s - 2.5s response

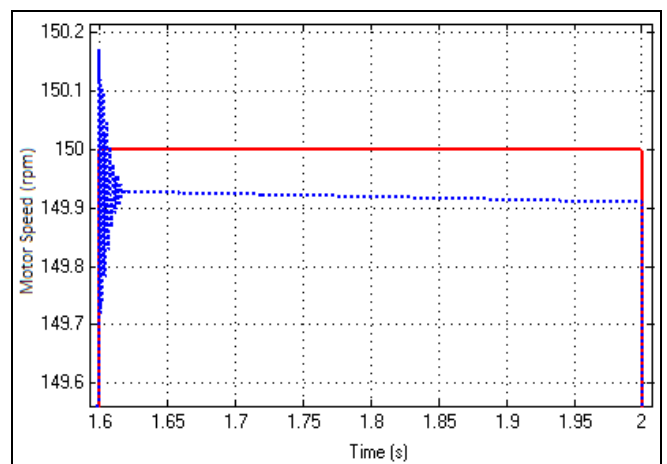


Fig. 13. SEPIC converter with PID controller 1.6s - 2.5s response

PI controlled system simulation results are shown in Figure 11, Figure 12 and Figure 13.

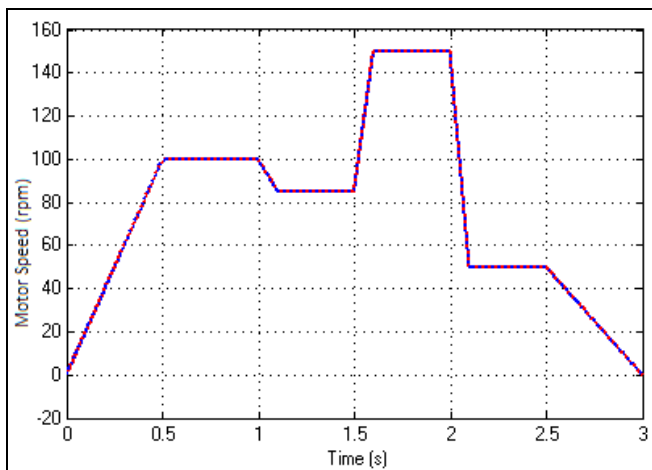


Fig. 11. SEPIC converter with PID controller 0s - 3s response

Fuzzy controlled system simulation results are shown in Figure 14, Figure 15 and Figure 16.

The Fuzzy logic control method can easily be applied SEPIC converters. In this study, the voltage applied to the motor to control the speed PMDC must be changed over time, and reduces both can increase the SEPIC converter voltage converter types are selected. Converter control conventional PI, PID and Fuzzy Logic control were performed separately.

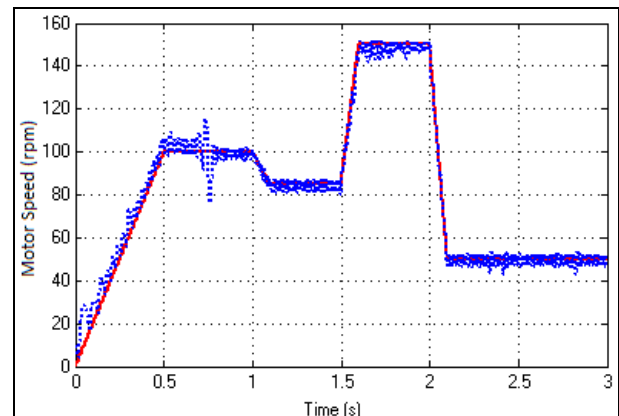


Fig. 14. SEPIC converter with Fuzzy logic controller 0s - 3s response

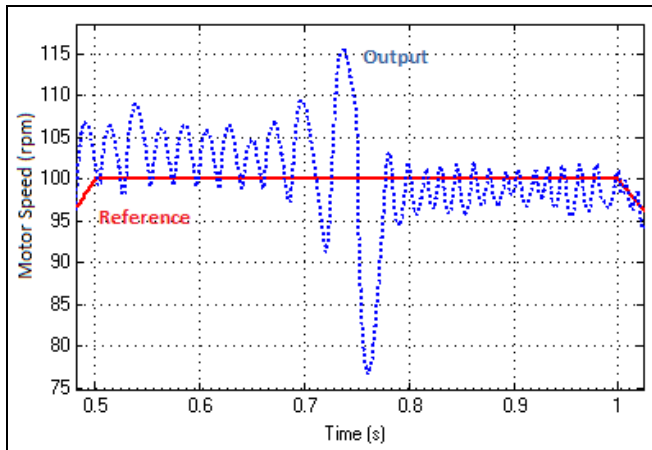


Fig. 15. SEPIC converter with Fuzzy logic controller 0.5s - 1s response

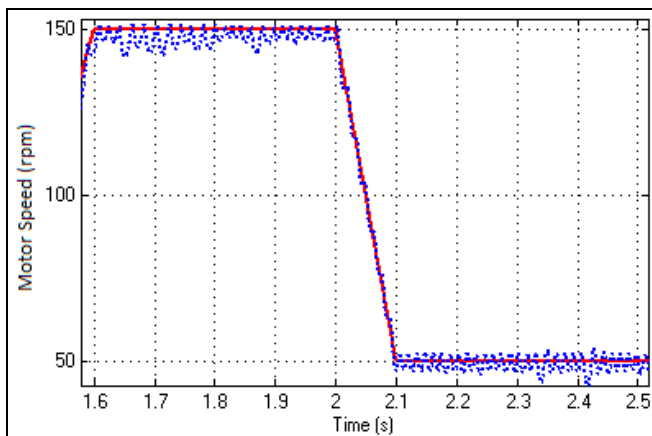


Fig. 13. SEPIC converter with fuzzy logic controller 1.6s - 2.5s response

The performance of a PMDC system with MATLAB/Simulink circuit is compared with a Sepic Converter driver designed in this study. The results show that the PID supervised system gives the best response. As shown in the graphs obtained under Fuzzy Logic control, there is a serious effect on system characteristics between fuzzy logic success due to control strategy and decision making, based on rule base. Similar to PID control, PI control provided better dynamic performance than fuzzy logic.

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